REMARKS

The new claims 31-32 are supported in the Detailed Description, in the second and third paragraphs under the heading Third Embodiment, reading, "a second region Y2 that includes the bonding pads BP and a first region Y1 excluding this region are defined ... the support substrate 1 located below the first region Y1 is removed, and the support substrate 1 remains in the area located below the second region Y2, that is, below the bonding pads ... the dielectric loss of a multiplicity of widely distributed elements can be reduced. The strength (rigidity) of the semiconductor device 300 is also maintained." Figs. 8 and 9 show this subject matter. The new claims are patentable for the reasons below. In response to the official action:

Claims 21, 22, 24, 25, 27, and 29 were rejected as being as anticipated by Sakai '165. This rejection is respectfully traversed.

Sakai Teaches Large Capacitance. In applied Fig. 12A, Sakai's transistors respond to sound rather than to light (as in the other embodiments) and are part of a microphone (col. 9, lines 5 and 21-27). In Fig. 12A, sound 193 impinges on an electret film 192 which is glued over an opening etched in the silicon layer 121. The p+ layer 122 is left in place (col. 8, line 52) and the surface of the layer 122 is silicided or metal-plated to be conductive, so that it acts as one plate of a capacitor "C", the other plate being the electret film 192 (col. 9, line 9). The electret film 192 includes a hole to let air in and out (col. 9, line 1), so the interior space is filled with air. As the sound 193 moves the film 192 to and fro, the interplate capacitance (between 122 and 192) changes to operate the circuit of Fig. 12B and vary the transistor current. Sakai has constructed a condenser-type microphone (capacitor microphone) based on the interplate capacitance between layers 122 and 192. The interplate capacitance is intentional.

Does Sakai suggest reducing the *stray* capacitance[1] of the transistor, located just above the capacitor? The Applicants think not.

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[1] The stray capacitance is defined as the capacitance between the transistor and ground.

First, placing any large grounded conductor near to an object increases the capacitance of that object,[2] and Sakai does exactly that. Sakai's layer 122 is coupled to the transistor gate (col. 8, lines 53-54 and Fig. 12B) but the electret 192 is grounded by being electrically connected to the substrate (col. 8, lines 66-67). The layer 122, being coupled to the transistor, will not much affect its capacitance (the stray capacitance of the source and drain will be affected, but not the gate). However, the electret 192—being large, metallic, grounded, and close to the transistor—will increase the stray capacitance substantially, and therefore it will increase the leakage current from the transistor at high frequencies.

Second, Sakai's microphone will be more sensitive if the capacitance between the layer 122 and the electret 192 is greater. Because a more sensitive microphone is a better microphone, Sakai inherently teaches a large capacitance, not a small one. A large capacitance means an electret plate 192 that is both larger and closer to the transistor (by the known properties of parallel-plate capacitors), and that means more stray capacitance and more leakage current.

Thus, Sakai teaches to *increase* the leakage due to capacitance, not to decrease it. The Examiner asserts that in Sakai "control of dielectric loss is sought" (page 3, line 10) but this is not taught by the reference itself and the Examiner refers to the Applicants' own specification for support, which is respectfully submitted to be legally incorrect.

SOI is Not Disclosed. Sakai discloses a silicon substrate 121, a silicon layer 122 above it, and SiO_2 above that.[3] The Examiner asserts that 123 is an SOI layer formed on the insulation layer 122, but 122 is "a p^+-type region" (col. 8, line 52) and the actual insulation layer is seen to be the layer 123.

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[2] By the method of images, an object at a distance *d* frm a grounded plate has just the capacitance of the same object a distance *2d* from another object of opposite charge.

[3] While the SiO_2 is not labeled in applied Fig. 12A, its diagonal hatching is the same as SiO_2 123 shown in various figures, such as Fig. 4 (col. 6, line 3), and the SiO_2 layer 222 in figures such as Fig. 13 (col. 9, line 46).

With respect, the claimed features "an SOI layer formed on top of the first insulation layer [and] a first element layer formed in a first-element area on the SOI layer" are not disclosed because there is no silicon *layer* above insulation layer 123 that has any "area" in which elements are formed; only the silicon elements themselves (124, 125,127) are formed there and there is no silicon is in between any of them.

The Element Layer. Furthermore, there is no "a second insulation layer formed on top of the first element layer; and at least one additional element layer formed on top of the second insulation layer" as claimed because 138 is metal wiring (col. 6, line 51) rather than an additional element layer as the Examiner asserts.

The Examiner asserts that 138 is an element layer because "it can be connected" to other components. However, (1) anything "can be connected" to anything else, so this does not define or distinguish in a meaningful way, and (2) the metal wiring is completely unlike the transistor, so that it cannot be "an additional" one of the transistor.

Bonding Pads. With respect, these are inferred rather than actually disclosed by the reference. The reference itself discloses only the wiring 138, and there is no distinction in the reference between the wiring that is above the transistors and the wiring that is not; neither is there, according to the reference, any region "surrounding the first-element area" as the Applicants claim. With respect, the Examiner is reading a feature into the reference.

It is noted that Reedy (applied in a different rejection) shows bonding pads 601 but not any groove or cavity, so there is no teaching from that reference about bonding pad location.

Double Application. The rejection applies Sakai's metal 138 to anticipate two different claim features: the additional elements, and the bonding pads. Such a double application is believed to be legally incorrect. One feature in the reference cannot anticipate two different features in the claim when the two claim features are dissimilar.

Claims 1-3, 6-7, 9, 23, 30, and 32 were rejected as being as anticipated by Sakai in view of Reedy. This rejection is respectfully traversed.

The Examiner asserts that it would have been obvious to make Sakai's silicon substrate out of Reedy's sapphire so as to combine electronic and optical components and to permit light to pass through the substrate (page 4, line 14). This is respectfully traversed.

Sapphire Would Be Useless in Sakai. First, Sakai teaches directly *against* permitting light to pass through the substrate, except in the case in which the transistors are to act as photoreceptors. If they are to act as just transistors (i.e. act normally), then, according to Sakai they must be *shielded* from light, and Sakai uses an opaque layer to allow light to reach some transistors and not others, so that some are controlled by the light and others are not. In Fig. 4, the p+ layer 122 is to block light and it is placed under any MOS transistor that is not to be affected by light (col. 7, lines 3-9). This teaching is also in the Abstract and Sakai's claim 1. Conversely, layer 122 is removed from under the MOS transistor of Fig. 4 so that the light 131 can reach the transistor above it, but this transistor "is used as a photoreceptor device" (col. 6, line 17) to produce current proportional to the amount of light (col. 6, lines 22-25). Increasing the transparency by using sapphire would cause more interference with the regular transistors, and would not improve the situation for the photoreceptor transistors because the substrate is already removed from under those. There would be no advantage for either type of transistor.

As to the applied microphonic embodiment of Fig. 12A, the substrate is again removed under the transistors and no the microphone would not be improved by using sapphire.

Optical+Electronic. Second, as to combining optical and electronic components, this asserted advantage is not supported by either citation or by argument, nor is it applied to the facts of either reference. Sakai itself discloses both light sensors and electronic devices (e.g. the microphone) but does not combine them; it presents them as alternate embodiments, and thereby teaches against combining optical and electronic components. With respect, combination is not suggested. Reedy presents a way to combine electronic and optical components (col. 4, lines 52-

56) in the case where there is some reason to combine them; it does not advocate arbitrary combinations, and a microphone like that of Sakai's applied Fig. 12A does not need any optical feature because it responds to sound.

A Cavity Would Be Useless to Reedy. As noted above, sapphire would be useless in Sakai, which teaches removing the substrate to let in light. Conversely, Reedy uses transparent sapphire to let light in and does not need any cavity or groove, unlike Sakai that has a silicon substrate and therefore needs a groove to let the light in. And if Reedy were to make a condenser microphone like Fig. 12A of Sakai, then no solid—including sapphire—would work in place of air.

The Deficiencies of Sakai Are Not Made Up By Reedy. It is noted that Reedy does not disclose the features which are lacking from Sakai. For example, the claimed additional element layer is not found in either one of the references, so that no combination would reach the instant claims, even if combination were suggested (not admitted).

Claims 4 and 8 were rejected as being as anticipated by Sakai in view of Reedy and Eda '057. This rejection is respectfully traversed.

Inductors. The Examiner has not presented any citation, or any argument based on common knowledge, to show why an inductor would be useful for either Sakai or Reedy. How would an inductor contribute to Sakai's microphone of applied Fig. 12A, or to Reedy's opto-electronic device? What advantage would have motivated the person of ordinary skill to combine the references?

Eda only mentions inductors as one type of passive component and does not teach their use for any specific purpose or disclose any advantage.

Eda Teaches Away. Eda shows the inductor 5' displaced *away* from the cavity under the crystal resonator 2/7 in Fig. 7; the same is true in Fig. 6 where inductor 5 is shown.[4] Thus, Eda does not disclose a groove below a target element and it teaches that an inductor should be put over a *solid* substrate, not over a groove as the Applicants claim. Therefore, even if the references were combined (not admitted), the person of ordinary skill would have put an inductor into the structure of Sakai *away* from the microphone cavity. Therefore, no combination (not admitted obvious) would reach the instant claims.

The advantage disclosed by the Applicants' specification ("When the groove G is formed below the first region X1, the dielectric loss of the inductor 21 which is the target element is reduced") is not suggested by *any* of the references.

It is noted that Eda does not disclose the features discussed above which are lacking from Sakai and Reedy. No combination would reach the instant claims, even if combination were suggested (not admitted).

Claims 26 and 28 were rejected as being as anticipated by Sakai in view of Eda. This rejection is respectfully traversed on the same grounds as claims 4 and 8 above.

In summary, the references teach putting a device over a substrate cavity for various purposes, but do not suggest to reduce stray capacitance or dielectric loss by this structure.

The New Claims. Claims 31 and 32 are exemplified by Figs. 8 and 9. The entire non-bonding pad area (Y1 in the drawing) is full of elements which are especially to benefit from lower dielectric loss, and other elements. Nothing in the prior art suggests such a structure, in which the thickened surrounding bonding pad region mechanically reinforces the substrate. None of the applied references shows a cavity under non-selected as well as selected devices.

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[4] The Examiner applies Fig. 6, but cites text describing Fig. 7.

As discussed above, Sakai discloses cavities only for light transmission or creating a microphone capacitor, and there is no suggestion of exending these cavities in area. In fact, the applied microphone embodiment would be impossible with the Applicants' claimed structure because there would be nothing to support the edges of the electret 192. As noted, not bonding pads are seen in Sakai, so the claimed subject matter would, again, be impossible.

Reedy discloses no cavity at all.

Eda discloses a cavity only for use with a quartz resonator (Fig. 7 and col. 13, line 23). The cavity appears to be provided only so that the lower contact 7 can reach the crystal 2 and for no other reason. There is no disclosure of or suggestion toward the Applicants' claims.

For the reasons above, withdrawal of the rejections and allowance of the claims are requested.

Respectfully submitted,

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